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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/749,815	12/30/2003	Andrew S. Grover	42.p18167	9370

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EXAMINER	
WALTER, CRAIG E	

ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 02/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/749,815	GROVER, ANDREW S.	
	Examiner	Art Unit	
	Craig E. Walter	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 July 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings were received on 30 December 2003. These drawings are deemed acceptable for examination.

Specification

2. The abstract of the disclosure is objected to because of the following:

All extraneous marks should be removed from the abstract (i.e. "Attorney Docket 42.P181167").

Correction is required. See MPEP § 608.01(b).

Claim Objections

3. Claims 2, 6-7, 9, 13, 15 and 17-19 are objected to because of the following informalities:

As for claims 15 and 17-19, it is of the Examiner's opinion that Applicant intended these claims to depend directly on claim 14 (as these three claims recite a system rather than a medium as recited in claim 8). The claims will be further treated on their merits based on this presumption.

As for claims 2, 6-7, 9, 13, 15 and 19, the phrase "the hard disk" should be changed to "a hard disk" else the phrase would lack antecedent basis.

As for claims 7, 13 and 19, the phrase "events the produced" should be changed to "events that produced".

Appropriate correction is required.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

4. Claims 8-13 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. More specifically, the machine readable medium as recited in these claims is directed to a combination of statutory subject matter (i.e. ASIC's and EEPROM's), and non-statutory subject matter such as carrier waves and signals). See paragraph 0021 (all lines) on page 8 of the specification.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-2, 6-9, 13-15 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fortin et al., hereinafter Fortin (US PG Publication 2004/0003223 A1, in further view of Douglis et al., hereinafter Douglis (US Patent 5,481,733).

As for claims 1, 8 and 14, Fortin teaches a system comprising of:

a processor (Fig. 2, element 120);

a non-volatile cache coupled to the processor (Fig. 2, flash memory 200 can be located as a separate component (as shown by element 202) which is coupled to the processor via the system bus (element 121) – paragraph 0030, all lines). Also note, the flash memory (element 200) can also serve as a cache for the hard disk (paragraph 0036, lines 1-11 – Powering down of the system is decreased by storing data that is being sent to the disk for storage that the OS can not control such as an application writing to the disk to the flash memory for storage, hence reducing the number writes to the disk) – In other words, the flash is used as a cache by the system to reduce the access burden of the hard disk; and

a machine readable medium having stored thereon a set of instructions (the system memory as illustrated in Fig. 2, element 130, contains RAM and ROM sections which contain the OS, application programs, boot code, etc. which are used by the system to execute all system functions).

Though Fortin teaches storing configuration data in the non-volatile memory, he fails to teach the configuration data as comprising historical hard disk performance data.

Douglis teaches a method for managing the power distributed to a disk drive in a laptop computer, wherein a state table is stored in a memory, the memory being used to store performance data of the hard disk drive. Based upon a history of disk accesses

by a user, the number of transitions between each pair of states is counted and stored in memory. The information is used to predict a future period of inactivity in order to conserve power to the disk drive (see abstract).

It would have been obvious to one of ordinary skill in the art at the time of the invention for Fortin to further include Douglis's method of saving historical performance data into the cache memory of his own system used to store configuration data. By doing so, Fortin would benefit by having a means of storing the historical data of his hard disk, in order to spin down the hard drive during predicted periods of inactivity, hence conserving power of his computer system as taught by Douglis (col. 8, lines 15-25). Note, though Douglis's teaches his system as being applied to a laptop computer, it is well known to one of ordinary skill in the art that power conservation is valuable to many different computing systems, not just to a laptop computer environment.

As for claims 2, 9 and 15, Fortin teaches the non-volatile cache as being a cache for the hard disk (the flash memory (element 200) can serves as a cache for the hard disk (paragraph 0036, lines 1-11 – Powering down of the system is decreased by storing data that is being sent to the disk for storage that the OS can not control such as an application writing to the disk to the flash memory for storage, hence reducing the number writes to the disk) – In other words, the flash is used as a cache by the system to reduce the access burden of the hard disk).

As for claim 6, Douglis teaches using the historical hard disk performance data to implement a power management policy of the hard disk (the predicated period based on

historical accesses by the user ultimately leads to spinning down the disk in order to put it in low power mode (see abstract)).

As for claims 7, 13 and 19 Douglis teaches the historical hard disk performance data consists of data identifying events the produced a spin-down of the hard disk and a period of time thereafter before the hard disk was spun up. Douglis teaches spinning down a hard disk drive when it is unlikely to be accessed in the near future (col. 8, lines 15-25). A prediction is made based on the past history of disk activity, which is stored in the memory. If the most likely time for the disk to be accessed is greater than a preset threshold, then the disk is spun down (col. 8, lines 38-50). In the case of this power down, historical data is recorded (i.e. period of inactivity) which indicates that the power down occurred because the inactivity data stored indicates the threshold has been exceeded. The method Douglis teaches includes quantizing the periods of inactivity into states, therefore periods of activity, and inactivity can be recorded to more efficiently power down the system (col. 8, lines 52-63). The states that are recorded to include predicting when to spin the drive back up based on the predicated next access (col. 10, lines 46-59). In other words, the system works to anticipate how long the drive should stay powered down before its spun back up based on the historical data.

It would have been obvious to one of ordinary skill in the art at the time of the invention for Fortin to further include Douglis's method of saving historical performance data into the cache memory of his own system used to store configuration data. By doing so, Fortin would benefit by having a means of storing the historical data of his hard disk, in order to spin down the hard drive during predicted periods of inactivity,

hence conserving power of his computer system as taught by Douglis (col. 8, lines 15-25).

6. Claims 5, 12, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combined teachings of Fortin and Douglis as applied to claims 1, 8 and 14 above, and in further view of Sanada et al., hereinafter Sanada (US PG Publication 2001/0002173 A1). Though the combined teachings of Fortin and Douglis meet all the limitations of the base claims, they fail to further include the non-volatile memory consisting of a thin film electronic memory.

Sanada however teaches a semiconductor storage device and production method thereof wherein he specifically teaches manufacturing a flash memory via thin film processing techniques (paragraph 0071, all lines).

It would have been obvious to one of ordinary skill in the art at the time of the invention for Fortin to include his cache memory as consisting of thin film. By doing so, he would benefit by having a more optimized memory that is capable of uniform data erase in a group of memory cells with a reduced number of cell in which the data erase is excessively performed as taught by Sanada (paragraph 0039, all lines).

7. Claims 3-4, 10-11 and 16-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combined teachings of Fortin and Douglis as applied to claims 1, 8 and 14 above, and in further view of Chou et al., hereinafter Chou (US PG Publication 2005/0055481 A1).

Though the combined teachings of Fortin and Douglis meet all the limitations of the base claims, they fail to further teach the memory include a form factor of a Mini

Peripheral Component Interconnect Express (mini-PCI express) card, and interface. It is worthy to note Fortin does discuss his flash memory as a separate component such as a PC slot card, just not implemented as a mini-PCI express – see paragraph 0017, lines 1-9.

Chou however teaches a Flash drive/reader with serial-port controller and flash-memory controller mastering a second RAM-buffer bus parallel to a CPU bus. In his disclosure, Chou teaches connecting a system CPU to flash-controller, which accesses an attached flash memory, which is further connected to serial engine (see Fig. 4). This connection can be implemented in part by a mini-PCI Express (paragraph 0055, all lines). Also note, a Mini-PCI express card, must inherently posses a Peripheral Component Interconnect Express interface in order to function (i.e. communicate with the system).

It would have been obvious to one of ordinary skill in the art at the time of the invention for Fortin to further include a mini- PCI Express to his flash memory component (depicted in Fig. 2, element 202). By doing so, Fortin would be able to exploit the benefits of increased data throughput via the buffering and second data bus as taught by Chou (paragraph 0024, all lines).

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Craig E. Walter whose telephone number is (571) 272-8154. The examiner can normally be reached on 8:30a - 5:00p M-F.

9. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (571) 272-4210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

10. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Craig E Walter
Examiner
Art Unit 2188

CEW

2/13/06

MANO PADMANABHAN
SUPERVISORY PATENT EXAMINER